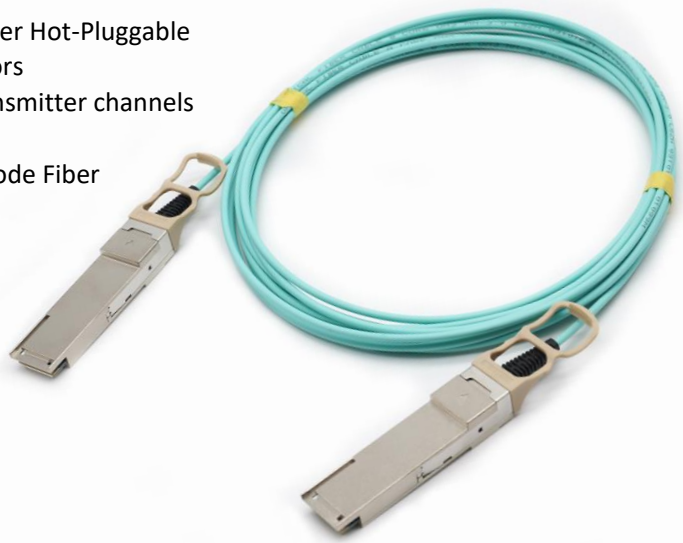
400Gb/s QSFP-DD Active Optical Cable Hot Pluggable, +3.3V, 850nm VCSEL, Multi mode PQSFP-DD56-AOCx

Features



- 8x53Gbps PAM4 transmitter and PAM4 receiver Hot-Pluggable
- 850nm VCSEL transmitters, PIN photo-detectors
- Internal CDR circuits on both receiver and transmitter channels
- Compliant with QSFP-DD MSA, CMIS
- Maximum link length of 70m on OM3 Multimode Fiber (MMF) and 100m on OM4 MMF with FEC
- Power Supply :+3.3V
- Low Power consumption<10W
- Operating case temperature Range:0~ 70°C
- RoHS compliant

Applications

- IEEE 802.3cd 200GBASE-SR4

Description

PeakOpical's 400G QSFP-DD Active Optical Cable is designed for 2x 200 Gigabit Ethernet Applications, links reach up to 70m (OM3) or 100m (OM4) over Multi-Mode Fiber (MMF) with FEC. This high-performance module integrates eight data lanes in each direction with 8x 26.5625GBd. Each lane can operate at a data rate up to 53.125Gbps using a nominal wavelength of 850nm. The electrical interface uses a 76-contact edge type connector.
The 400G QSFP-DD Active Optical Cable incorporates PeakOptical's proven circuit and VCSEL technology to provide reliable long life, high performance, and consistent service. It is compliant with the Common Management Interface Specification (CMIS).

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit
Storage Temperature	T_S	-40		+85	°C
Case Operating Temperature	T_A	0		70	°C
Maximum Supply Voltage	Vcc	0		3.5	V
Relative Humidity	RH	0		85	%

Electrical Characteristics (TOP = 0 to 70 °C, VCC = 3.135 to 3.465 Volts)

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Supply Voltage	Vcc	3.135		3.465	V	
Supply Current	Icc			3	A	
Power Consumption	P			10	W	
Data Rate	R	-	425		Gb/s	
Input differential impedance	R_{in}	90	100	110	Ω	1
Output differential impedance		90	100	110	Ω	1
Differential input voltage swing	ΔVin,pp	600	800	1000	mVp-p	
Differential output voltage swing	ΔVout,pp	200		900	mVp-p	
Bit Error Rate	BER			2.4E-4	-	2

Note:

1. Connected directly to TX data input pins and RX data output pins.
2. PRBS31Q@26.5625GBd. Pre-FEC.

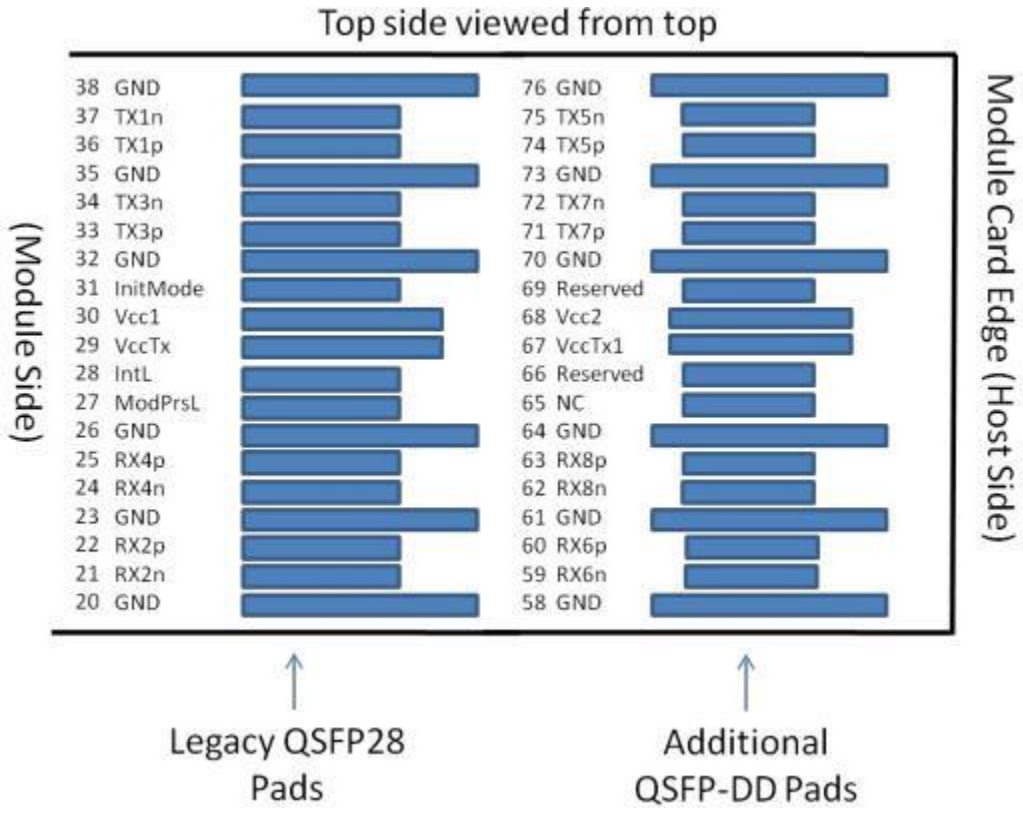
Optical Characteristics (TOP = 0 to 70°C, VCC = 3.135 to 3.465 Volts)

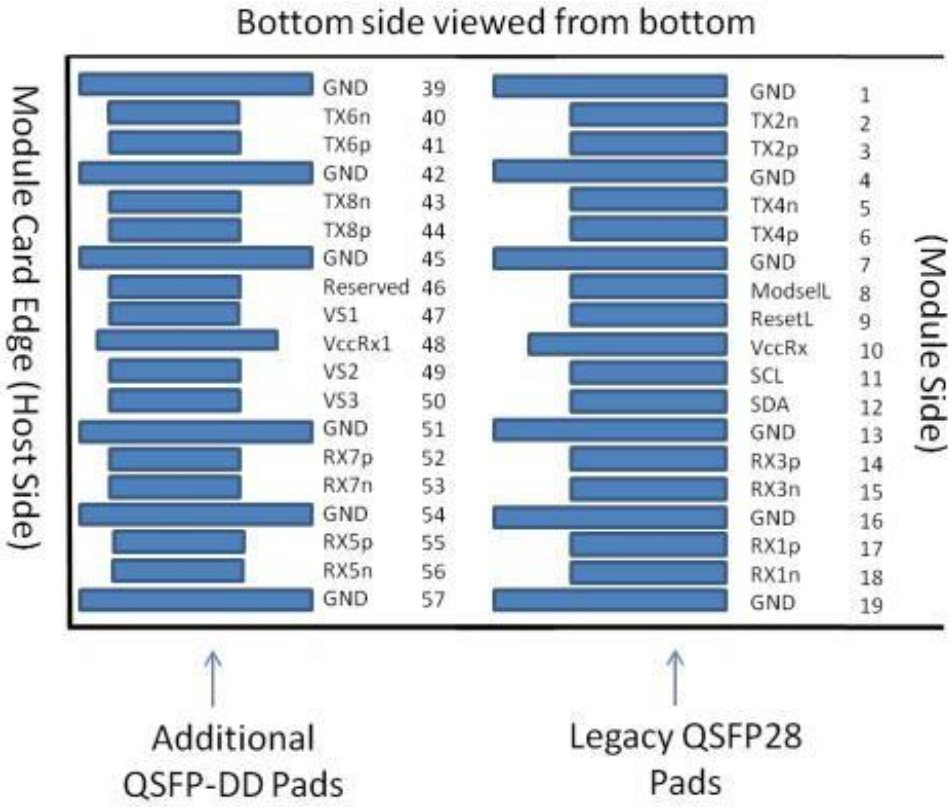
Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Transmitter Section:						
Center Wavelength	λt	840	850	860	nm	
spectral width	△λ			0.6	nm	
Average Optical Power	Pavg	-6.5		+4	dBm	1
Extinction Ratio	ER	3.0			dB	1
TDECQ, each lane	TDECQ			4.5	dB	1
Laser Off Power	Poff			-30	dBm	
Receiver Section:						
Center Wavelength	λr	840	850	860	nm	
Receiver Sensitivity in OMAout	RXsen			(-6.5,-3.4)	dBm	2
Maximum Average power at receiver , each lane input				4		
Minimum Average power at receiver , each lane input		-8.4				
Los Assert	LOS_A	-9.5		-	dBm	
Los Dessert	LOS_D			-7.5	dBm	
Los Hysteresis	LOS_H	0.5			dB	

Note

1. Average power figures are informative only, per IEEE Std 8023cd_D3p5.
2. Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC.

Pin Assignment





Pin Function Definitions

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	For Future Use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Note 1: QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently.Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

Note 3: All Vendor Specific, Reserved and No Connect pins may be terminated with 50ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads.Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by3A,3B.

Block Diagram

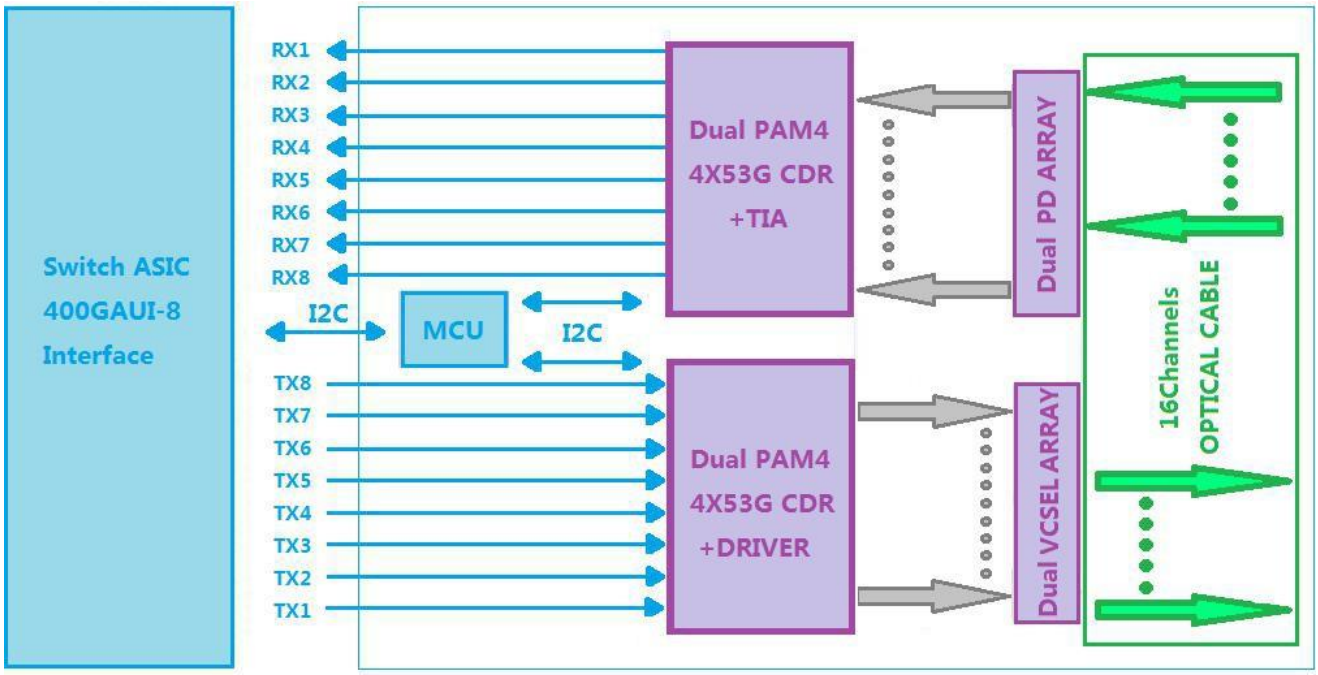


Figure 1. Block Diagram

Diagnostic Monitoring Interface

Digital diagnostics monitoring function is available on all QSFP DD products. A 2-wire serial interface provides user to contact with module.
This subsection defines the Memory Map for a CMIS Module used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all CMIS devices. The interface has been designed largely after the QSFP-DD memory map. The memory map has been changed in order to accommodate 8 electrical lanes and limit the required memory space. The single address approach is used as found in QSFP-

DD. Paging is used in order to enable time critical interactions between host and module.

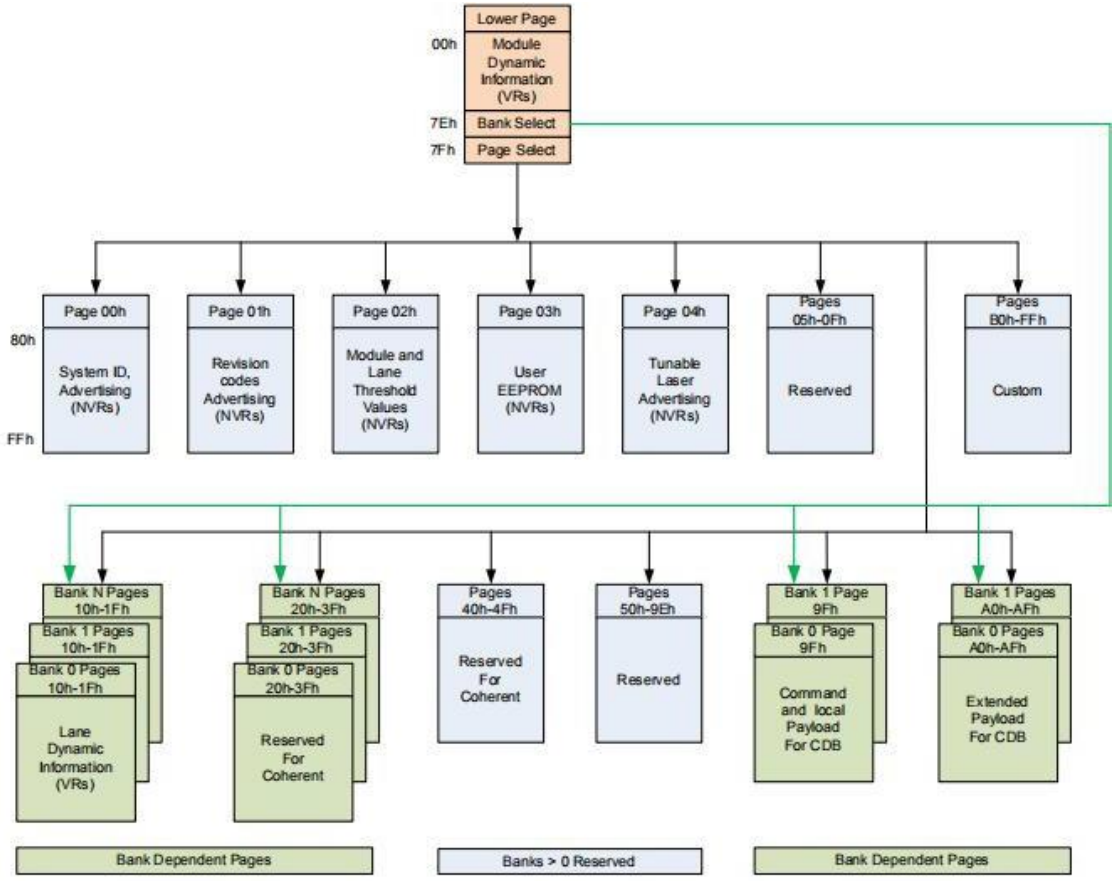


Figure 2-1. QSFP-DD Memory Map

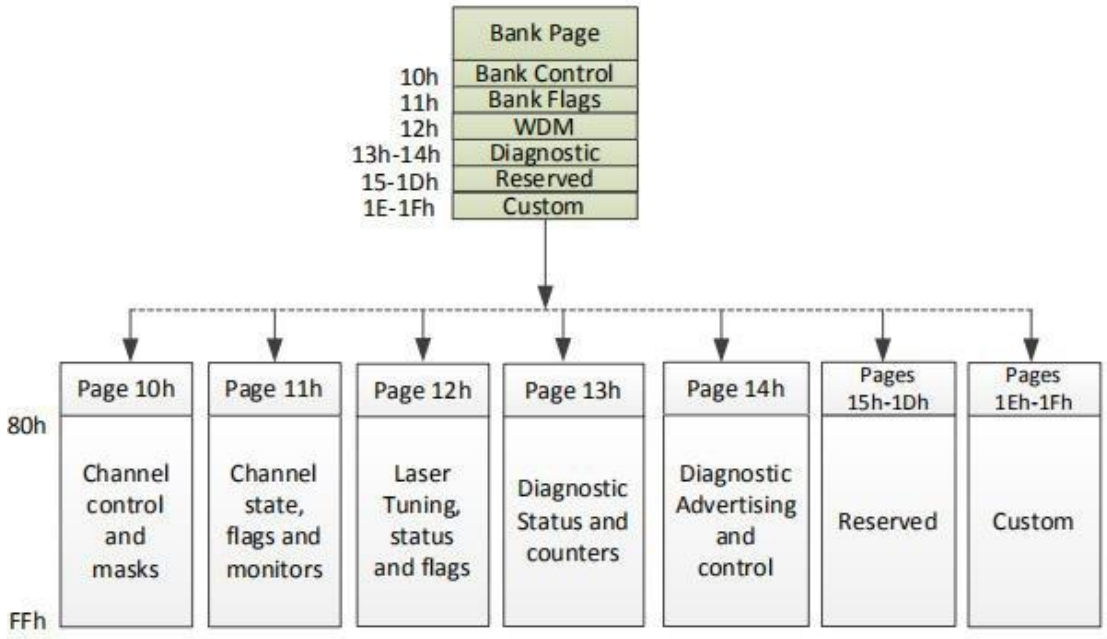


Figure 2-2. Blank Page Memory Map

Mechanical Dimensions